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(72) Inventors: SCHOBER, Joachim, H.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). SCHEUCHER, Heimo; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). HUBMER, Paul; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

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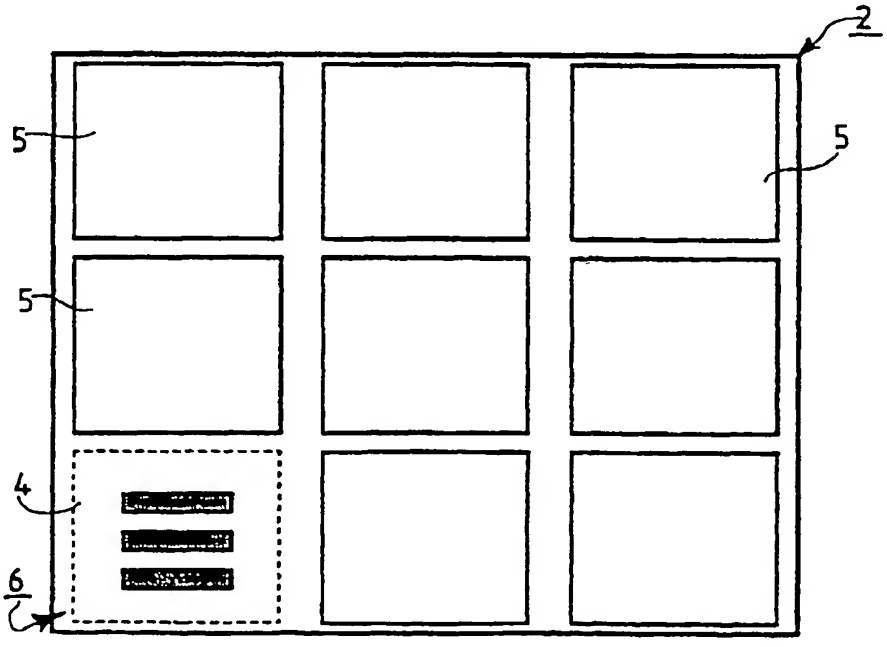
(54) Title: SEMICONDUCTOR WAFER WITH PROCESS CONTROL MODULES



(57) Abstract: A semiconductor wafer (1) has a multitude of chips (5), of which chips (5) each one of a given number of chips (5) is situated in one of a multitude of adjacent exposure fields (2), and further has process control modules (4) which are each arranged in an exposure field (2), namely each in place of at least one chip (5).

WO 02/069389 A2

Semiconductor wafer with process control modules

The invention relates to a semiconductor wafer having a multitude of chips, of which chips each one of a given number of chips is situated in one of a multitude of adjacent exposure fields, and having process control modules which are each arranged in a given area on the semiconductor wafer.

Such a semiconductor wafer has been marketed in several variants and is consequently known.

In a variant of such a known semiconductor wafer the given areas, in each of which a process control module is located, are formed by so-called drop-in areas which contain so-called alignment markers, which are reference or positioning structures by means of which the semiconductor wafer can be aligned with respect to an exposure mask in the course of the fabrication of the semiconductor wafer. This variant has the disadvantage that there are only a very small number of process control modules, i.e. only two or three of such process control modules, per semiconductor wafer, which has the drawback that as a result of the small number of process control modules these process control modules cannot detect or recognize flaws at locations of the semiconductor wafer which lie comparatively far from these process control modules.

Another variant of the known semiconductor wafer has a larger number of process control modules but the process control modules are arranged in the so-called dicing paths, which dicing paths extend between the chips, which are arranged in rows and columns. Owing to the presence of the process control modules in these dicing paths it is necessary to make these dicing paths comparatively wide in order to accommodate the process control modules. As a result of this, the dicing paths are unnecessarily wide, which is a waste of space. For such process control modules arranged at the location of the dicing paths reference may also be made to the patent document US 5,990,488 A, i.e. to the variant of a semiconductor wafer shown in Fig. 2 of said patent document and elucidated in the corresponding description.

In a further variant of a known semiconductor wafer a process control module is provided in the area of each chip of the semiconductor wafer. In practice, such a variant

may be considered only when the chips are large-area chips, for which the fact that each chip has a separate process control module is less significant.

It is an object of the invention to avoid the restrictions and drawbacks of the known variants of a known semiconductor wafer and to realize an improved semiconductor wafer.

In order to achieve the aforementioned object a semiconductor wafer in accordance with the invention has characteristic features in accordance with the invention, in such a manner that a semiconductor wafer in accordance with the invention can be characterized in the manner defined hereinafter, namely:

A semiconductor wafer having a multitude of chips, of which chips each one of a given number of chips is situated in one of a multitude of adjacent exposure fields, and having process control modules which are each arranged in a given area on the semiconductor wafer, in which the given areas are formed by the exposure fields, and in which each process control module takes the place of at least one chip.

Owing to the provision of the characteristic features in accordance with the invention a satisfactory compromise is achieved between, on the one hand, a maximal number of process control modules, in order to guarantee a maximal detection accuracy for incorrectly fabricated areas of a semiconductor wafer in accordance with the invention, and, on the other hand, a minimal number of process control modules, in order to lose a minimal semiconductor wafer area usable for chip fabrication. A further advantage is obtained in the case of large semiconductor wafers with very small chips, i.e. roughly speaking in the case of semiconductor wafers having a diameter of, for example, 200 mm and chips having a chip area of less than 2.0 mm^2, because the individual exposure fields can be identified very easily, i.e. even with the naked eye, which greatly facilitates finding a specific chip with the aid of the provided process control module. This is useful not only during a manually and visually performed inspection of a semiconductor wafer but particularly during the automatic further processing of the chips provided on the semiconductor wafer. This is because during the automatic further processing the process control modules provided in the exposure fields can be used as a kind of coarse grating in order to position a device for the manipulation of the individual chips of the semiconductor wafer, for example a so-called pick-and place device, after which said device can be positioned within a previously approached exposure

field with the aid of other positioning means. This ensures in a highly reliable manner that an erroneous removal of a chip from a semiconductor wafer is precluded.

With a semiconductor wafer in accordance with the invention it has proved to be very advantageous when a process control module is present in each of at least 25 % of all the exposure fields and the process control modules are disposed at equal distances from one another. Such an embodiment has proved to be advantageous during tests which have been conducted, because such an embodiment yields the desired result with a comparatively small amount of space being required for the process control modules and in spite of this guarantees a high detection reliability as regards the detection of defective or imperfectly fabricated areas of the semiconductor wafer.

With a semiconductor wafer in accordance with the invention it has proved to be particularly advantageous when a process control module is present in each exposure field. This ensures a particularly high detection reliability.

With a semiconductor wafer in accordance with the invention it has further proved to be particularly advantageous when all the process control modules in the exposure fields are each situated at the same location. The centers of the exposure fields should then be regarded as a preferred location. This is particularly advantageous in view of a simple detection of the location of the process control modules and in view of a simple cooperation with the process control modules.

The aforementioned aspects as well as further aspects of the invention will be apparent from the example of an embodiment described hereinafter and will be elucidated with the aid of this example.

The invention will be described in more detail hereinafter with reference to an embodiment which is shown in the drawing by way of example but to which the invention is not limited.

Fig. 1 shows a semiconductor wafer which is an embodiment of the invention in a highly diagrammatic manner, which semiconductor wafer has a multitude of exposure fields.

Fig. 2 shows an exposure field of the semiconductor wafer of Fig. 1 to a substantially larger scale than Fig. 1.

Fig. 1 shows a semiconductor wafer 1. The semiconductor wafer 1 comprises a multitude of chips. A given number of chips of this multitude of chips is situated in one of a

multitude of adjacent exposure fields 2, which are each shown diagrammatically as a rectangle in Fig. 1. Fig. 2 shows such an exposure field 2.

In English-language jargon such exposure fields are referred to as "reticles". In the present case, the semiconductor wafer 1 has two so-called drop-in areas, which in known manner serve for positioning the semiconductor wafer 1 and at least one exposure mask during the fabrication of the semiconductor wafer 1.

The semiconductor wafer 1 has further been provided with process control modules, which are each arranged in a given area on the semiconductor wafer 1, which is not apparent from Fig. 1 but which visible in Fig. 2.

In the semiconductor wafer 1 the given areas in which a process control module is present are formed by the exposure fields 2. Fig. 2 shows such a process control module 4 in broken lines to mark the difference with respect to the chips 5 present in the exposure field 2. As is apparent from Fig. 2, a process control module 4 has been provided in the reticle 2 in place of a chip 5. This applies to all the exposure fields 2 in which a process control module 4 has been provided in place of a chip 2. In the semiconductor wafer 1 shown in Figs. 1 and 2 a process control module 4 is present in each exposure field 2, but this is not necessarily so. The process control modules 4 are arranged in the exposure fields 2 in such a manner that all the process control modules 4 are situated at the same location within an exposure field 2. In the case of the semiconductor wafer 1 shown in Figs. 1 and 2 all the process control modules 4 are situated in the front-left corner areas 6 of the exposure fields 2 as is shown in Figs. 1 and 2. However, this is not strictly necessary because alternatively the process control modules 4 may be situated at any other location in the exposure fields 2, preferably a location in the center of the exposure field 2.

It is to be noted once more that it is not strictly necessary to provide a process control module 4 in each exposure field 2. It is also possible to provide a process control module 4 in each of only 50 % or 25 % of the exposure fields, but in that case it also advantageous if the process control modules 4 are situated at equal distances from each other with respect to two mutually perpendicular coordinate directions, which two mutually perpendicular coordinate directions are shown as two dash-dot lines 7 and 8 in Fig. 1. Furthermore, it is to be noted that the process control modules 4 need not be provided in place of only one chip 5 but may also be provided in place of two or more chips 5 if this is effective, which is so in the case of chips 5 of a particularly small area.

CLAIMS:

1. A semiconductor wafer (1) having a multitude of chips (5), of which chips (5) each one of a given number of chips (5) is situated in one of a multitude of adjacent exposure fields (2), and having process control modules (4) which are each arranged in a given area on the semiconductor wafer (1), in which the given areas are formed by the exposure fields (2), and in which each process control module (4) takes the place of at least one chip (5).

2. A semiconductor wafer (1) as claimed in claim 1, in which a process control module (4) is present in each one of at least 25 % of all the exposure fields (2), and in which the process control modules (4) are situated at equal distances from each other with respect to two mutually perpendicular coordinate directions (7, 8).

3. A semiconductor wafer (1) as claimed in claim 2, in which a process control module (4) is present in each exposure field (2).

4. A semiconductor wafer (1) as claimed in claim 1, in which all the process control modules (4) are each situated at the same location (6) in the respective exposure fields (2).

1/1

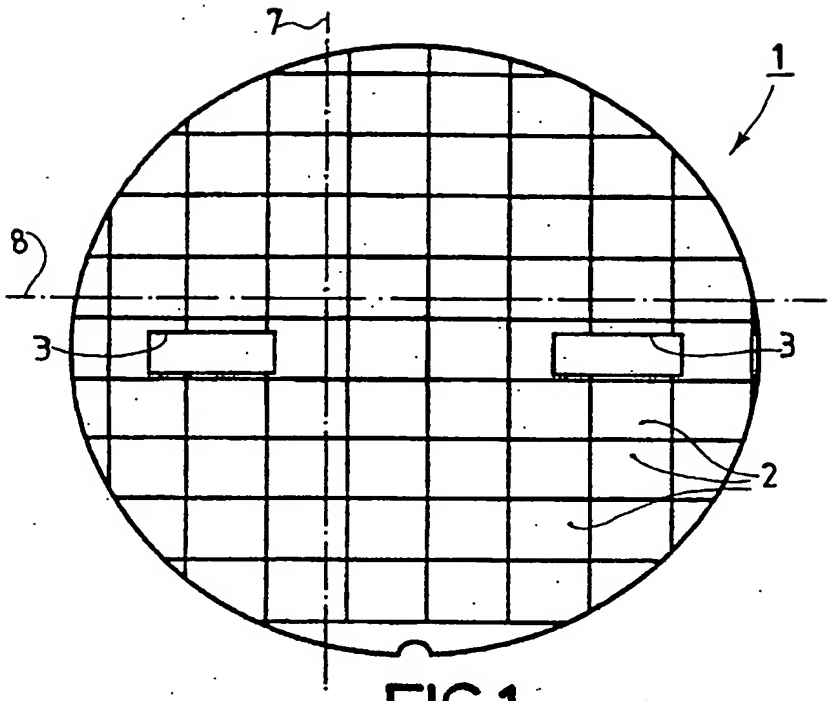


FIG.1

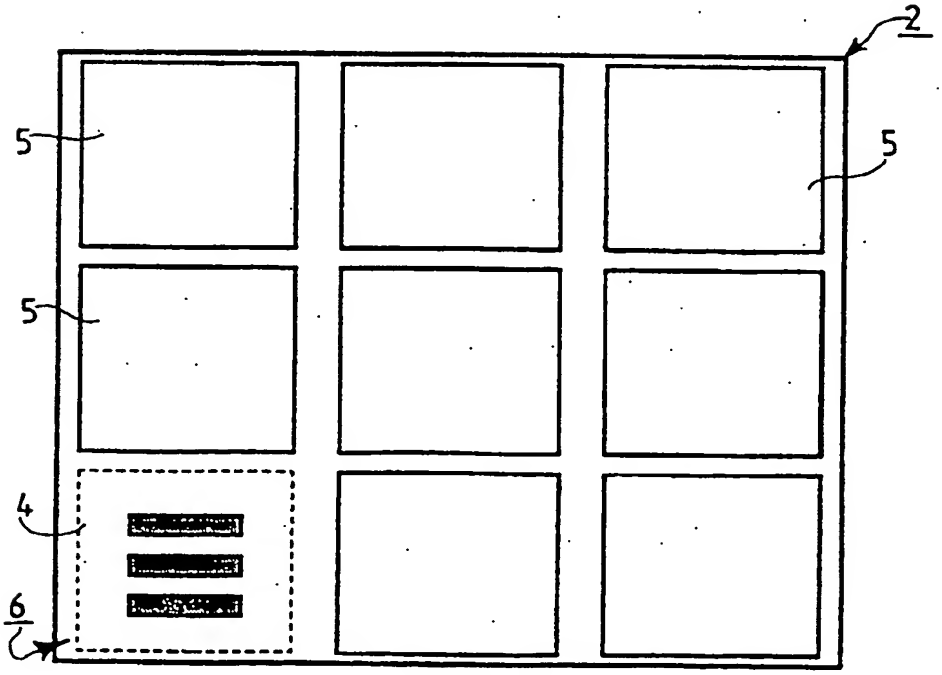


FIG.2

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(74) Agent: WEBER, Helmut; Internationaal Octrooibureau B.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

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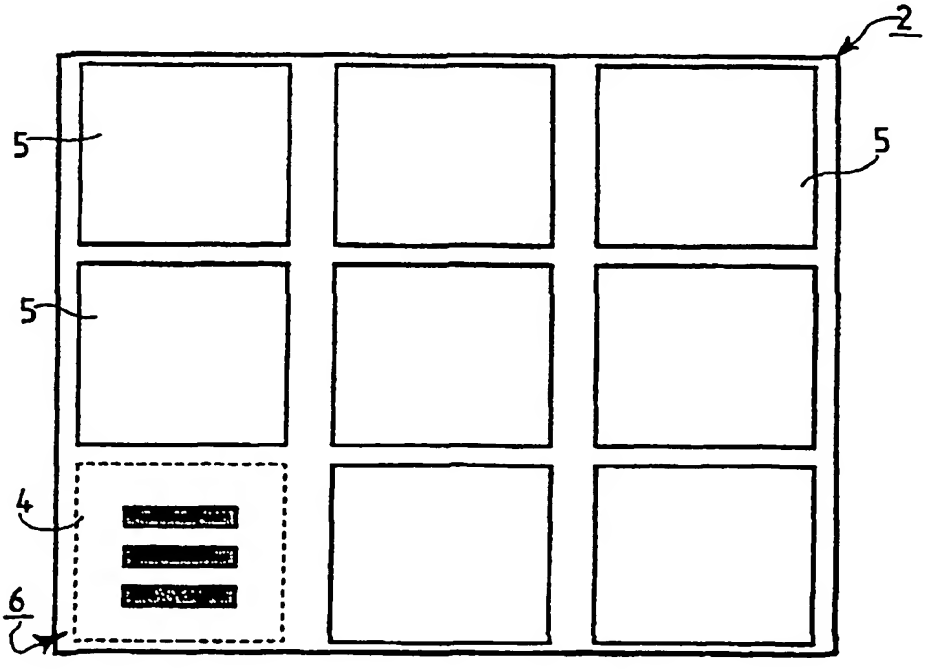

(57) Abstract: A semiconductor wafer (1) has a multitude of chips (5), of which chips (5) each one of a given number of chips (5) is situated in one of a multitude of adjacent exposure fields (2), and further has process control modules (4) which are each arranged in an exposure field (2), namely each in place of at least one chip (5).

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A. CLASSIFICATION OF SUBJECT MATTER
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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 007, no. 087 (P-190), 9 April 1983 (1983-04-09) -& JP 58 014137 A (FUJITSU KK), 26 January 1983 (1983-01-26) abstract	1-4

☐ Further documents are listed in the continuation of box C.

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° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 February 2003	21/02/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Prohaska, G

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/IB 02/00318

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 58014137 A	26-01-1983	JP 1646643 C	13-03-1992
		JP 3006649 B	30-01-1991

⑲ 日本国特許庁（JP）　　⑪ 特許出願公開

⑫ 公開特許公報（A）　　昭59—94418

⑤1Int. Cl.³　識別記号　庁内整理番号
H 01 L 21/30　Z 6603—5F

⑬公開　昭和59年(1984)5月31日

発明の数　1
審査請求　未請求

（全 2 頁）

⑤4半導体装置

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熊本市八幡町100番地九州日本電気株式会社内
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⑦1特　願　昭57—203402
⑦2出　願　昭57(1982)11月19日

明　細　書

1. 発明の名称

半導体装置

2. 特許請求の範囲

半導体装置製造においてフォトレジスト工程の目合露光工程に使用される位置合せパターンが半導体素子片間に配置されている事を特徴とする半導体装置。

3. 発明の詳細な説明

この発明は半導体装置の構造に関するものである。

従来、半導体装置の製造工程は熱酸化拡散処理工程とフォトレジスト・エッチング工程の繰り返しであり、フォトレジスト工程とは半導体基板表面に感光樹脂剤を塗布し目合・露光工程においてフォトマスクのパターンを焼き付け転写する工程であるが、このパターンの出来ばえを確認するための位置合せパターンがある。年々半導体装置の縮少化・高集積化が進むにつれて、工程も複雑になり、フォトレジスト工程も増加した為、フォトレジスト工程で使用される位置合せ用パターンの半導体素子片（ペレット）内の占有率も大きくなってきた。しかしながら、この位置合せパターンは、各フォトレジスト工程のフォトレジストパターンの出来ばえを確認するのに絶対に不可欠なものであり、今後該パターンが削除されるのは考えられない事であり、いかに該パターンの半導体素子片内占有率を小さくするかが考えられてきた。

この発明の目的はフォトレジスト工程の目合露光工程に使用される位置合せパターンを半導体素子片外へと配置する事を提供する事にある。

この発明の半導体装置は半導体装置製造においてフォトレジスト工程の目合露光工程及びフォトレジストパターンの出来ばえ（ズレなど）をチェックするために使用される位置合せ用パターンが半導体素子片外に配置されている事を特徴としている。

次に、この発明の一実施例につき図を用いて説明する。

第１図はこの発明の一実施例を説明するための半導体基板の平面図である。

従来の半導体装置は第２図に示すように、半導体素子片１内にフォトレジスト工程の目合・露光工程で使用される位置合せ用パターン２～１０は、まず最初に土台となる位置合せ用パターン２～６が半導体装置製造の最初の工程で形成され、各フォトレジスト工程を通過する度に、位置合せ用パターン２～６内に各フォトレジスト工程の位置合せパターン７～１０が位置合せされる。その為、工程の複雑化が進むとフォトレジスト工程も増加し位置合せ回数も増すため、位置合せ用パターンの数も多くなり、半導体素子片内に占める位置合せパターンの割合も大きくなる。そこで、本実施例（第１図）では、該位置合せ用パターンを半導体素子片間のスクライブ線１１へ配置した。

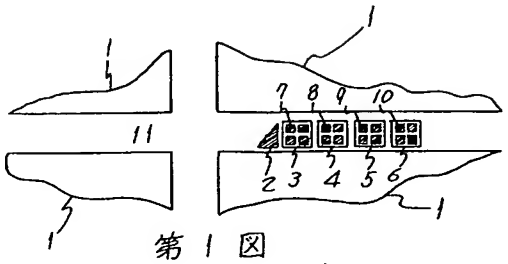
この実施例によれば、位置合せ用パターンを半導体素子片外に配置した事により半導体素子片内の開いた場所へ、他の素子回路を増やす事ができる。

4. 図面の簡単な説明

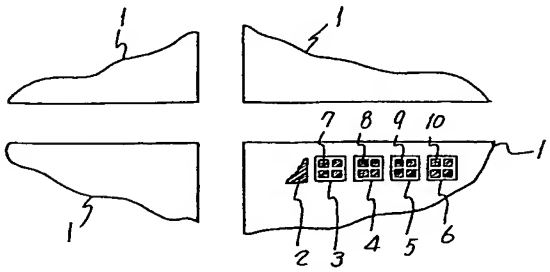
第１図は本発明の一実施例を示す半導体装置の平面図であり、第２図は従来の半導体装置を示す平面図である。

尚、図において、１……半導体素子片（ペレット）、２～１０……位置合せ用パターン、１１……スクライブ線。

代理人　弁理士　　内　原　　晋



第１図



第２図

INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L G03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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Y	PATENT ABSTRACTS OF JAPAN vol. 008, no. 209 (E-268), 22 September 1984 (1984-09-22) -& JP 59 094418 A (KIYUUSHIYUU NIPPON DENKI KK), 31 May 1984 (1984-05-31) abstract; figures 1,2	1-4
Y	US 2003/211700 A1 (LEUNG FRANK C ET AL) 13 November 2003 (2003-11-13) paragraph '0055!; figure 1	1,2
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[X] Further documents are listed in the continuation of box C.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 February 2005	07/03/2005

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Bakker, J

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INTERNATIONAL SEARCH REPORT

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PCT/IB2004/052724

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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A	EP 1 284 499 A (BROADCOM CORPORATION) 19 February 2003 (2003-02-19) process control monitor in scribe line paragraph '0034! - paragraph '0035!; figure 4	1,2
A	US 4 642 672 A (KITAKATA ET AL) 10 February 1987 (1987-02-10) column 4, line 43 - column 5, line 9; figure 4	2

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Information on patent family members

Inte [redacted] l Application No
PCT/IB2004/052724

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